Appl. No.: 10/689,382 Docket No.: DB001064-000

Preliminary Amdt. Dated: 7 October 2004

Amendments to the Specification:

On page 1, please amend paragraph [0001] as follows:

[0001] The present application is related to U.S. Patent Application Serial No.
10/689,345 [[]] entitled "Method for Load Balancing a Line of Parallel
Processing Elements" filed [[]]-(DB001066-000, Micron no. 02-1267) 20
October 2003, U.S. Patent Application Serial No. 10/689,312 [[]] entitled
"Method for Using Extrema to Load Balance a Loop of Parallel Processing Elements"
filed [[]]-(DB001067-000, Micron no. 02-1297) 20 October 2003, U.S. Patent
Application Serial No. 10/689,336 [[]] entitled "Method for Load Balancing a
Loop of Parallel Processing Elements" filed [[]]-(DB001068-000, Micron no. 02-
1298) 20 October 2003, U.S. Patent Application Serial No. 10/689,355 [[]]
entitled "Method for Using Filtering to Load Balance a Loop of Parallel Processing
Elements" filed [[]]-(DB001061-000, Micron no. 02-1296) 20 October 2003,
U.S. Patent Application Serial No. 10/689,365 [[]] entitled "Method for Load"
Balancing an N-Dimensional Array of Parallel Processing Elements" filed [[]]
(DB001062-000, Micron no. 02-1295) 20 October 2003, and U.S. Patent Application
Serial No. 10/689,280 [[]] entitled "Method of Obtaining Interleave Interval for
Two Data Values" filed [[]]-(DB001065-000, Micron no. 02-1268) 20 October
<u>2003</u> .

On page 7, please amend paragraph [0037] as follows:

[0037] The reader desiring more information about the hardware shown in FIGs. 1 and 2 is directed to UK Patent application No. 0221563.0 (serial no. not yet assigned) entitled "Control of Processing Elements in Parallel Processors" filed 17 September 2002, (Mieron no. 02-1604) which is hereby incorporated by reference. Details about the PEs may also be found in UK Patent Application No. 021562.2 entitled "Host Memory Interface for a Parallel Processor" filed 17 September 2002, (Mieron no. 02-0703) which is hereby incorporated by reference.